This memorandum is written to inform Laboratory personnel that ECAP, a general purpose electronic circuit analysis program, is available for their use; describe the program; and provide instructions concerning its use. Section I is a general explanation of the function of the program, Section II contains a description of the software with which the ECAP user must be familiar, and the step-by-step computing procedure is detailed in Section III. Wherever possible in Section III, examples rather than lengthy discussions are used to demonstrate proper procedure.

No attempt has been made to duplicate completely the information in the ECAP Operators Manuals references (a), (b), and (c). Instead, an attempt has been made to present sufficient information to permit the reader to program circuit analyses after reading this document. When specific problems arise, however, the Operators Manuals should be consulted.

SECTION I: PROGRAM DESCRIPTION

The Electronic Circuit Analysis Program (ECAP) is a general purpose program which allows USL engineers to utilize the computer facilities at the Laboratory to analyze electronic circuits. The International Business Machines Corporation and the Norden Division of United Aircraft Corporation jointly developed ECAP, and TRW Systems converted it for use on USL's IBM 704 computer.

ECAP is really a combination of three analysis programs:

(1) a DC Analysis Program,
(2) an AC Analysis Program, and
(3) a Transient Analysis Program

For the DC Analysis Program the circuit must be described using...
resistors, independent voltage sources, dependent current sources, and independent current sources. The computer will calculate and print out all the voltages and currents, power dissipation, worst case voltages, sensitivities, and standard deviations if so directed by program control cards. In addition, certain intermediate results such as current, impedance, and admittance matrices will be printed out if requested by the engineer. The circuit parameters may be modified, permitting the engineer to study the effects of component variations on circuit performance.

Only resistors, capacitors, inductors (including mutual inductors), independent voltage sources, independent current sources, and dependent current sources can be used to describe a circuit for an AC analysis. This program will compute and print out at a single frequency all voltages, currents, element power dissipations, current matrices and admittance matrices if so desired. As with the DC Analysis Program the circuit parameters (including frequency) may be varied.

The Transient Analysis Program requires that the circuit be modeled with resistors, capacitors, inductors; DC independent and time-varying independent voltage sources; DC independent, time-varying independent and dependent current sources; and logical switches. Circuit parameters can be automatically altered when branch currents reverse direction through the use of the Logical Switch. With the Transient Analysis Program all node voltages and element currents are printed out as a function of time.

ECAP is a very useful design review tool. The DC Analysis Program can be used to evaluate DC bias currents and voltage; determine stress ratios; perform worst case, statistical, or sensitivity analysis of circuits. A frequency analysis can be conducted by use of the AC Analysis Program to obtain open-loop frequency response data. With the Transient Analysis Program and piece-wise linear models of non-linear devices, actual circuit performance as a function of time can be duplicated. As a result, biasing of circuits involving non-linear devices can be studied, the step response of a circuit can be analyzed, rise and fall times can be measured and the output of a non-linear circuit for various combinations of inputs can be computed using the Transient Analysis Program.

SECTION II: PROGRAMMING SOFTWARE

The USN/USL ECAP user must familiarize himself with only two printed forms. They are the Compilation/Check-Out/Production Request and the Fortran Coding Form and Data sheet. Both are available in the USL Computing Center.

The Compilation/Check-Out/Production Requests properly completed for each type of analysis, are shown in figures 1, 2, and 3. Because the request form is returned to the ECAP user following the execution of each analysis, the request is filled-in only once for each type of analysis. The information for items 1, 2, 4, and 5 is unique to each ECAP user; the other items on the form need not be altered.
Figure 4 is a Fortran Coding Form and Data Sheet. The information in the heading is self-explanatory and the body of the form is used to describe the punched cards required by the ECAP user.

The punched cards necessary to utilize ECAP are grouped into six categories:

1. Time Cards,
2. Comment Cards,
3. Command Cards,
4. Data Cards,
5. Solution Control Cards, and

Computer Center Personnel punch the Time Card (see figure 5) from the Compilation/Check-Out/Production Request. When submitted with the program deck, it will be retained by the Computer Operator.

Comment Cards are characterized by a C in column 1 and a message in the data field which extends from column 7 to column 72. These cards serve no useful programming function; the message is simply reproduced on the output data sheet. Cards with only a C in column 1 cause line spaces in the print-out.

Each analysis program deck should begin with Comment Cards which identify the output data. The format for these Identification Cards has been established by the author and has proved useful to the author and computer center personnel.

Three identification cards are used:

1. A Program Description Card,
2. A Circuit Description Card, and
3. A Date Card.

The information for these cards is demonstrated in figure 6. The first card identifies the program, the computer, the program user, his code, and his extension. The circuit Description Card identifies the circuit being analyzed and the third card identifies the run number, and date.

There are five cards in the Category Command Cards. They are:

1. AC Analysis,
2. DC Analysis,
3. Transient Analysis,
4. Execute, and
5. Modify Cards.

The data for these cards is shown if figure 7. Only one Analysis
Card is used per program deck. Modify cards may only be used with the AC and DC Analysis Programs. An Execute Card is paired with the Analysis Card and every Modify Card.

There are five types of Data Cards:

(1) B-Cards,
(2) T-Cards,
(3) M-Cards,
(4) S-Cards, and
(5) Source Cards.

The Standard Branch written into ECAP is shown in figure 8. The directions of positive currents and the polarities of positive voltages are shown on the figure. Reversed directions and polarities must be indicated by negative values on the Data Cards.

The B-Card is used to describe the initial and final nodes, the linear element, the time-invariant independent voltage source, the time-invariant independent current source, and initial conditions. Figure 9 demonstrates the relationship between the B-Card and the Standard Branch.

The Branch number is written in columns 1 through 5 of the data card and the remainder of the data must appear in columns 7 through 72. The node numbers are put on the data card in sequence, the initial node first. Therefore, the directions of positive currents and the polarities of positive voltages are established by the user's selection of the initial node. Ground nodes are assigned the number 0. Following the node numbers, the parameter values appear separated by commas. Initial conditions (i.e., voltage across capacitors and currents through inductors at the initial time of a Transient Analysis) are established by EQ and IO statements. Note that any Fortran coding of numbers is acceptable to describe parameter values. For those not familiar with the coding of scientific notation, $1.2 \times 10^3$ is written in Fortran 1.2E3.

The T-Card describes the dependent current source in each branch. Like the B-Card, Columns 1 through 5 are used only for the number of the dependent source. The control and source branch numbers, in that order, and the current gain which relates the element current of the control branch to the source current appear in the data field. Examples of the use of the T-Card may be found in figure 10.

The mutual inductance between two branches containing inductors is described by the M-Card. The format of this card is similar to that of the T-Card. However, the order of the branch numbers is unimportant. The application of M-Cards is demonstrated in figure 11.

The logical switch operation is controlled by the S-Card. Like the other cards discussed so far, the S-Card number is put in columns
1 through 5. The element current of a branch is sensed and when that current is zero or negative, the switch is off; when the current is positive, the switch is on. As the state of the switch changes, the values of circuit parameters may be changed. Look at the Fortran statement for the S-Card in figure 12. The S-Card causes the element current of branch 2 to be sensed. When the current changes, branches 2, 3, and 4 will be affected. Initially the state of the switch is off (i.e., the current in branch 2 is zero or negative). With S1 in the off state, the resistance of branch 2 is 500, the capacitance of branch 3 is \(2 \times 10^4\), and the beta of the dependent current source is 100. When S1 goes on (i.e., branch 2 current goes positive), the resistance of branch 2 goes to 550, the capacitance of branch 3 goes to \(3 \times 10^4\), and the beta of Ti goes to 125. Note that the beta of Ti is altered by having the switch action affect branch 4 (the control branch), not branch 1 (the source branch). Should the current return to zero or go negative, the parameters would return to their initial values.

To describe time-varying independent voltage and current sources, three types of Source Cards are used:

(1) Non-Periodic,
(2) Periodic, and
(3) Sinusoidal.

The Non-Periodic Source Card data is shown on line 2 of figure 13. Columns 1 through 5 of the card define the type of source (current or voltage) and the number of the branch in which it is positioned. In the data field, the number of time steps between changes in source values appears in parentheses, and the voltages or currents at each increment of time beginning at start time appear separated by commas. The Time Step on line 3 indicates the interval at which circuit performance is computed. A linear change in amplitude between time increments is assumed and the value of the final entry is maintained until final time is reached. The number of voltage entries is limited to 126.

Figure 14 demonstrates a Periodic Source Card. Except for the addition of a P in the data field to designate a periodic function, the data entries are identical to those of the Non-Periodic Source Card. The first and last value of voltage or current should be equal because the function is periodic. As for the Non-Periodic source the maximum number of entries is 126.

A Sinusoidal Source Card is described in figure 15. Columns 1 through 5 are used to describe the type of source and branch number as with the Non-Periodic and Periodic Source Cards. In the data field, however, SIN is used to indicate that a sinusoidal source is desired and the period in seconds is put in parentheses. The peak value, the DC average value, and the initial time shift follow, separated by commas.
For an AC Analysis, B-Cards, T-Cards, and M-Cards; for a DC Analysis, only B-Cards and T-Cards; and for a Transient Analysis, B-Cards, T-Cards, S-Cards, and Source Cards are used.

Continuation Cards may be used if the data is in excess of the data field of one card. A Continuation Card is characterized by an asterisk in column 6. The data field of the Continuation Card can then be considered an extension of the previous Data Card.

The number of Data Cards is limited to:

200 B-Cards (limited to 50 inductors if M-Cards are used)
200 T-Cards, and
200 S-Cards.

In addition, the circuit must contain no more than 50 nodes.

The data cards used with Modify-Execute Card pairs have a modified format. First, the data field of the card need only describe the parameter to be changed. Second, multiple variations of a parameter may be written into one statement which defines the initial value, the number of steps (in parentheses), and the final value. Examples of these Data Cards can be found in figure 16. No more than 50 parameter changes in one parameter modification are allowed.

Solution Control cards are unique to the type of Analysis being performed. Figures 17, 18, and 19 lists the Fortran statements for Solution Control Cards.

If the AC Analysis Program is being used there is only one Solution Control Card and this card must appear in the program card deck to specify frequency. When the Frequency Card is used to control the initial computation, only one value of frequency may be specified. When the Frequency Card is used with a Modify-Execute Card Pair, a single value, and arithmetic progression, or a geometric progression may be specified. See figure 17. For an arithmetic progression the initial value, the number of evenly spaced steps, and the final value are written. The number of steps must appear in parentheses with a plus sign. For a geometric progression, the ratio is specified in parentheses instead of the number of steps. The lack of a plus sign indicates a geometric progression.

Three Solution Control Cards may be used if a DC Analysis Program is in use. If the Sensitivity Card appears in the card deck, the partials and sensitivities of each node voltage with respect to each resistance, beta, and source value is computed and printed out. If the Worst Case Card appears in the deck, the worst case minimum, worst case maximum, and nominal node voltages for each node specified
on the Worst Case Card are printed out. If no node numbers are written all node voltages will be printed out. For this computation the minimum and maximum values or the tolerances, in addition to the nominal parameter values, must be specified. See figures 9 and 10 for examples of how to specify the extremal values. The Standard Deviation Card causes the standard deviation of each node voltage to be printed out. For this computation, the standard deviation values of the circuit parameters are specified with the same format that the minimum and maximum values are specified for a Worst Case Analysis.

When the Transient Analysis is being run, ten Solution Control Cards may be used. See figure 19. The Time Step Card must appear in every transient analysis. However, if any of the other 9 cards are omitted, the values listed in figure 20 are assumed. The Output Interval Card specifies the number of Time Steps between data printouts. When the Equilibrium Card is entered in the card deck, a solution is obtained with the inductors in the circuit replaced by short circuits and capacitors by open circuits. The values of open and short circuits are specified with the appropriate Solution Control Cards. The 1-ERROR, 2-ERROR, and 3-ERROR Cards control the acceptable magnitude of the sum of the nodal current unbalances, the accuracy of the switch acutation time printed out, and the value of the time steps immediately after an initial condition solution. Reference (a) should be consulted if it is desired to use these ERROR cards.

The Output Specification Cards allow control by the ECAP User of the data printed out. See figure 21.

For the AC and DC Analysis Programs:

1. node voltages (NV) (VOLTAGES),
2. element voltages (CV),
3. branch voltages (BV),
4. element currents (CA),
5. branch currents (BA),
6. element power dissipation (BP), and
7. miscellaneous outputs (MI) (MISCELLANEOUS)

can be printed out. The various voltages and currents are designated on the diagram of the Standard Branch (figure 8). Element power is the product of element voltage and element current. Miscellaneous outputs are current and impedance matrices for AC Analyses; and admittance, current, and impedance matrices for DC Analyses.

For the Transient Analysis Program, the only data permitted to be printed out is:

1. node voltages (NV) (VOLTAGES) and
2. element currents (CA) (CURRENTS).
SECTION III: COMPUTING PROCEDURE

The author recommends the computing procedure established in this section of the memorandum. Although other procedures will work as well, the author has demonstrated that delays and errors are minimized by following the steps outlined here.

To demonstrate the suggested computing procedure, the bias, frequency response, and response to a square wave of the circuit diagramed in figure 22 will be determined. The DC circuit will be subjected to a Transient Analysis to determine bias conditions; the worst case bias conditions will be determined using the DC Analysis Program once the nominal bias conditions have been established; the frequency analysis will be performed on the circuit with the AC Analysis Program; and finally, the Transient Analysis Program will be used to determine the step response of the circuit.

Figure 23 is the ECAP DC Circuit Diagram. This diagram is drawn directly from the Standard Circuit Diagram (figure 22) and differs very little from a standard dc equivalent circuit. Note, however, that care has been taken to arrange the circuit elements such that a Standard Branch (figure 8) appears between every pair of nodes, to indicate the direction of element currents, and to number the nodes and branches using consecutive numbers. Ground nodes are numbered 0.

Models for non-linear devices should be carefully selected. There is no one model which meets all applications. This is especially true of transient models. The author urges each ECAP user to select a model which duplicates with sufficient accuracy the parameters which have the greatest effect on the particular outputs desired. The models in figures 24 and 25 were carefully chosen to be only as sophisticated as they need be. Because they duplicate the VBE-IB and VCE-IC characteristics of the 2N930 type transistor with sufficient accuracy to determine the bias points, the complex models in figure 24 were selected. However, the simple models diagramed in figure 25 adequately represent the V-I characteristics once the nominal bias points have been determined. The values of the parameters (voltage and resistance) in branches 9 and 11 are based on the results of the analysis using the models in figure 24.

To document the ECAP Data, a Compilation/Check-Out/Production Coding Form and Data Sheets must be filled in. Figures 26 and 27 show the Fortran sheets completed for the Transient Analysis of the DC Circuit. Note the difference between the letter Ø and the number 0, the letter I and the number 1.

To expedite the computation, the computer center personnel are assisted by the ECAP user. The completed forms are brought to the
Card Punch Operators' Room where they are date-stamped and left. The ECAP User is called when the cards have been punched and verified. Usually, this takes one day. When the user is called, he returns to the Card Punch Room to receive his original forms plus the punched cards. The cards are then assembled in the proper order:

1. Time Card
2. Identification (Comment) Cards,
3. Analysis (Command) Card,
4. Data Cards,
5. Solution Control Cards,
6. Output Specification Card,
7. Execute (Command) Card,

The cards are then submitted to the Computer Room with the Compilation/Check-Out/Production Request in front of the deck under the elastic band. The Production Log is filled-in as shown in figure 28 and the card deck is put in the "Production" box located in the Computer Center. The output data will usually be available in 4 hours.

The output data for the Transient Analysis of the DC Circuit may be found in Appendix A. The voltages are recorded on the ECAP DC Circuit Diagram in figure 23.

Once the bias points have been determined, the dc transistor models shown in figure 25 result and a Worst Case DC Analysis can be run.

Once again a Request Form (figure 2) and a Coding Form (figure 29) are completed and submitted to the Key Punch Operators. When the punched cards are returned, appropriate cards from the Bias Point Analysis are used to assemble a deck which results in the statements appearing on page B-1 of Appendix B. A check should be made to insure that the cards are in the proper order. The extra cards required for data modifications are put in the following order:

1. Modification (Command) Card,
2. Data Cards, and
3. Execute (Command) Card.

The dc output data appears in Appendix B.

Knowing the bias points, the ECAP AC Circuit Diagram (figure 30) and the Transistor Model Diagrams (figure 31) are drawn. An AC Analysis Request Form (figure 1) is completed and the circuit data is transferred to the Coding Forms. Modification of AC Analysis data require that the extra cards be put in the following order:

1. Modification (Command) Card,
2. Data Cards,
(3) Frequency (Solution Control) Card, and
(4) Execute (Command) Card.

The input data statements and the output data appear in Appendix C. The output data is plotted in figure 32.

To determine the response to a step input function, a transient analysis was run. The Transient Circuit Diagram and Transistor Models are shown in figures 33 and 34 respectively. The input step is shown in figure 35. The input and output data are recorded in Appendix D. The output response data is plotted in figure 36. It should be noted that the initial voltage across each capacitor is specified in the input data. In addition, it should be noted that it was necessary to exclude from the transient analysis the 60 microfarad capacitor in the power supply isolation network. Until this was done the accuracy of the current computations at node 5 was inadequate.

**SUMMARY**

This memo was written to introduce the Electronic Circuit Analysis Program to the reader. The author in no way pretends that this memo thoroughly covers the use of ECAP. On the other hand, it is hoped that after reading this memo, most engineers will be able to utilize the available computational tool without reading the IBM ECAP Users Manual (Reference (a)). However, if and when problems arise, or when additional information is needed, the appropriate reference or references listed in this memo should be consulted.

ECAP is a complex analysis program, especially useful as a design review tool. Breadboarding can be minimized or eliminated with proper use of this program.

*Alfred A. Filippini*

Electronic Engineer
LIST OF REFERENCES


(b) "Electronic Circuit Analysis Program (ECAP) for IBM 704 at USN/USL." 7423-6007-TO-000, TRW Systems, California, 6 December 1965, Contract No. NOw-65-0195-d, 119 pages.

(c) "7090/7094 ECAP," International Business Machines Corporation, New York, 18 pages.


CHECK-OUT/PRODUCTION REQUEST

A. Check-Out (2)  
B. Production (3)  

To Be Called

HRS. MIN. 20

1. Requestor: A. Filippini
2. Tel. Ext. No.: 470
3. Coded Job No.: 0678
4. Job Order No.: 1-654-00-00
5. Organization Code: 2134.4
6. Open Shop (X)  
   Closed Shop (X)
7. Fortran (X)  
   (or)
   S.A.P. (or)
8. Components Used
   a. Reader  
   c. Mag, Drum
   b. Printer  
   d. Punch

9. Sense Switches used:
   All assumed up unless checked.  
   SS 1, SS 2, SS 3, SS 4, SS 5, SS 6.

10. WRITE TAPE IDENTIFICATION

<table>
<thead>
<tr>
<th>Unit No.</th>
<th>Input</th>
<th>Output</th>
<th>CHECK APPROPRIATE BOXES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SYSTEM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>X</td>
<td>AC ANALYSIS PROGRAM</td>
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</tr>
<tr>
<td>3</td>
<td>X</td>
<td>INPUT CARDS</td>
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</tr>
<tr>
<td>4</td>
<td>X</td>
<td>OUTPUT TAPE</td>
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Program Steps and Procedures:
HPR 5,0 = Correct Halt  
HPR 6,0 = Bad ID Halt

NORMAL STOP HPR (0,1)

Special Instructions: BINARY TAPES IN HONEYWELL CABINET.

FIGURE 1: AC ANALYSIS REQUEST
# DC Analysis Request

**Requestor:** A. Filippini  
**Tel. Ext. No.:** 470  
**Coded Job No.:** 0679  
**Job Order No.:** 1-654-00-00  
**Organization Code:** 2134.4  
**Components Used:**
- a. Reader
- b. Printer
- c. Mag., Drum
- d. Punch

**Sense Switches Used:**
- SS 1
- SS 2
- SS 3
- SS 4
- SS 5
- SS 6

**WRITE TAPE IDENTIFICATION**

<table>
<thead>
<tr>
<th>Unit No.</th>
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<th>Output</th>
<th>WRITE TAPE IDENTIFICATION</th>
<th>CHECK APPROPRIATE BOXES</th>
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<td>2</td>
<td>X</td>
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</table>

**Program Stops and Procedures:**
- HPR 5,0 = Correct Halt
- HPR 6,0 = Bad ID Halt

**Special Instructions:**
- BINARY TAPES IN HONEYWELL CABINET.

**Figure 2:** DC Analysis Request
CHECK-OUT PRODUCTION REQUEST

1. Requester: A. Filippini
2. Tel. Ext. No.: 470
3. Coded Job No.: 0680
4. Job Order No.: 1-654-00-00
5. Organization Code: 2134.4
6. Open Shop: X (Closed Shop: )
7. Fortran: X
8. Components Used:
   - Reader: 
   - Mag. Drum: 
   - Printer: 
   - Punch: 
9. Sense Switches used: SS 1, SS 2, SS 3, SS 4, SS 5, SS 6
10. Special Instructions: BINARY TAPES IN HONEYWELL CABINET.

<table>
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<tr>
<th>Unit No.</th>
<th>Input</th>
<th>Output</th>
<th>WRITE TAPE IDENTIFICATION</th>
<th>CHECK APPROPRIATE BOXES</th>
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</thead>
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<td>SYSTEM</td>
<td>Save</td>
<td>Punch</td>
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<tr>
<td>2</td>
<td>X</td>
<td>TRANSIENT ANALYSIS PROGRAM</td>
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</tr>
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<td>X</td>
<td>INPUT CARDS</td>
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<td>X</td>
<td>OUTPUT TAPE</td>
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</tbody>
</table>

Program Stop and Procedures:
- HPR 5,0 = Correct Halt
- HPR 6,0 = Bad ID Halt
- NORMAL STOP HPR (0,1)

Special Instructions: BINARY TAPES IN HONEYWELL CABINET.

FIGURE 3: TRANSIENT ANALYSIS REQUEST
**FIGURE 5: TIME CARD**

<table>
<thead>
<tr>
<th>STATEMENT NUMBER</th>
<th>FORTRAN STATEMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ECAP, IBM 704, A FILIPPI (CODE 934-A, X 076)</td>
</tr>
<tr>
<td>2</td>
<td>DEMONSTRATION AMPLIFIER</td>
</tr>
<tr>
<td>3</td>
<td>RUN 1, 30 JUNE 1966</td>
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</table>

**FIGURE 6: FORTRAN STATEMENTS FOR IDENTIFICATION CARDS**

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<th>FORTRAN STATEMENT</th>
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<td>1</td>
<td>AC ANALYSIS 0678</td>
</tr>
<tr>
<td>2</td>
<td>DC ANALYSIS 0679</td>
</tr>
<tr>
<td>3</td>
<td>TRANSIENT ANALYSIS 0680</td>
</tr>
<tr>
<td>4</td>
<td>EXECUTE</td>
</tr>
<tr>
<td>5</td>
<td>MODIFY</td>
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**FIGURE 7: FORTRAN STATEMENTS FOR COMMAND CARDS**
FIGURE 8: THE STANDARD BRANCH
**Figure 9: Examples of B-Card Data**
FIGURE 10: EXAMPLES OF T-CARD DATA
FIGURE 11: AN EXAMPLE OF M-CARD DATA

FIGURE 12: AN EXAMPLE OF S-CARD DATA
FIGURE 13: AN EXAMPLE OF A NON-PERIODIC SOURCE CARD

FIGURE 14: AN EXAMPLE OF A PERIODIC SOURCE CARD
FIGURE 15: AN EXAMPLE OF A SINUSOIDAL SOURCE CARD

INDEPENDENT VOLTAGE SOURCES IN BRANCH B1 CHANGED TO 5V.

R = 6, 7, 8, 9, 10, 11, 12, 13, 14
  8 VALUES

BETA = 100, 125, 150, 175, 200
  4 VALUES

FIGURE 16: DATA FOR USE WITH MODIFY-EXECUTE CARDS
\[ f = 5 \text{ KHz} \]
\[ f = 5, 10, 15, 20, 25 \text{ KHz} \]
\[ f = 1, 2, 4, 8, \ldots, 128, 256 \text{ MHz} \]

**FIGURE 17: AC ANALYSIS SOLUTION CONTROL DATA**

**FIGURE 18: DC ANALYSIS SOLUTION CONTROL DATA**
### FIGURE 19: TRANSIENT ANALYSIS SOLUTION CONTROL DATA

<table>
<thead>
<tr>
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### FIGURE 20: ASSUMED SOLUTION CONTROL DATA

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FIGURE 21: OUTPUT SPECIFICATION DATA
FIGURE 22: STANDARD CIRCUIT DIAGRAM
FIGURE 23: ECAP DC DIAGRAM
FIGURE 24: TRANSISTOR 2N930 TRANSIENT MODELS

FIGURE 25: TRANSISTOR 2N930 DC MODELS
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**FIGURE 26: BIAS ANALYSIS DATA**
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<tbody>
<tr>
<td>1</td>
<td>S4 R=13,(12),FF</td>
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<tr>
<td>2</td>
<td>B14 N(3,4),R=266</td>
</tr>
<tr>
<td>3</td>
<td>T1 B(9,14),BETA=200</td>
</tr>
<tr>
<td>4</td>
<td>C Q2,3,N930</td>
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<tr>
<td>5</td>
<td>B15 N(3,9),R=11</td>
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<tr>
<td>6</td>
<td>B16 N(9,4),R=(1086,23.386),E=-0.65</td>
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<td>7</td>
<td>S5 B=16,(16),FF</td>
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<td>8</td>
<td>B17 N(9,7),R=(1086,5.26453),E=-0.62</td>
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<td>S6 B=17,(17),FF</td>
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<td>B13 N(9,4),R=(1086,3.74433),E=-0.66</td>
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<td>S7 B=18,(18),FF</td>
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<td>B8 N(7,4),R=100</td>
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<td>B19 N(7,5),R=(326,1)</td>
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<tr>
<td>14</td>
<td>S8 B=19,(19),FF</td>
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**FIGURE 27: BIAS ANALYSIS DATA**
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<th>Est. (Min)</th>
<th>Requestor</th>
<th>Remarks</th>
<th>PROC</th>
<th>Batch Input</th>
<th>Prop. in 204</th>
<th>Output Tape</th>
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<td>A. Felippes</td>
<td>ECAP TRANSFER</td>
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**FIGURE 28: PRODUCTION LOG**
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<td>R = 396E3 (.02)</td>
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<td>R = 100E3 (.01)</td>
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<td>R = 2.2E3 (.02)</td>
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<td>M(5,3)</td>
<td>R = 9.7E3 (.02)</td>
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<td>M(0,5)</td>
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<td>M(1,2)</td>
<td>R = 2.5, EF = 0.55</td>
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**FIGURE 29: DC ANALYSIS DATA**
FIGURE 30: ECAP AC CIRCUIT DIAGRAM
FIGURE 31: TRANSISTOR 2N930 AC MODELS
Figure 32: Demonstration Amplifier Gain Versus Driving Source Frequency
FIGURE 33: ECAP TRANSIENT DIAGRAM
FIGURE 34: TRANSISTOR 2N930 TRANSIENT MODELS

FIGURE 35: INPUT STEP FUNCTION
DEMONSTRATION AMPLIFIER
STEP RESPONSE

FIGURE 36
**APPENDIX A**

ECAP IBM 704 A FILLIPPII CODE 344.4 X 470

DEMONSTRATION AMPLIFIER

BIAS ANALYSIS

RUN 1 30 JUNE 1966

TRANSIENT ANALYSIS 0680

THE CIRCUIT ELEMENTS

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<th>Element</th>
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<td>B1</td>
<td>N(1*0)*R=390E3</td>
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<td>B2</td>
<td>N(4*1)*R=100F3</td>
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<td>B3</td>
<td>N(4*0)*R=2.2E3</td>
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<td>N(2*0)*R=47E3</td>
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<td>B5</td>
<td>N(5*3)*R=47E3</td>
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<td>B6</td>
<td>N(0*5)*R=220</td>
</tr>
<tr>
<td>E6</td>
<td>(1)*R=25</td>
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</table>

C1 2N930
B9 N(1*8)*R=1
B10 N(8*2)*R=(1E6+23.3E3)*E=-0.55
S1  B=10*(10)*OFF
B11 N(8*2)*R=(1E6+5.74E3)*E=-0.62
S2  B=11*(11)*OFF
B12 N(8*2)*R=(1E6+3.74E3)*E=-0.65
S3  B=12*(12)*OFF
B7  N(6*2)*R=100
B13 N(6*3)*R=(2E6+1)
S4  B=13*(13)*OFF
B14 N(3*6)*R=2E6
T1  B(9*14)*BETA=200

C2 2N930
B15 N(3*9)*R=1
B16 N(9*4)*R=(1E6+23.3E3)*E=-0.55
S5  B=16*(16)*OFF
B17 N(9*4)*R=(1E6+5.74E3)*E=-0.62
S6  B=17*(17)*OFF
B18 N(9*4)*R=(1E6+3.74E3)*E=-0.65
S7  B=18*(18)*OFF
B8  N(7*4)*R=100
B19 N(7*5)*R=(2E6+1)
S8  B=19*(19)*OFF
B20 N(5*7)*R=2E6
T2  B(15*20)*BETA=200

TIME STEP=1E-6
FINAL TIME=1E-6
PRINT VOLTAGES
EXECUTE

T = 0

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USL Tech Memo
No 2134.4-597-67

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APPENDIX B

ECEF 1174 A 470 A 597 CODE 340 40 X 470
DEMONSTRATION AMPLIFIER
EX 1 12 JULY 1966

DC ANALYSIS 0679

THE CIRCUIT ELEMENTS
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Worst Case Solutions for Node Voltages

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### T2
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### EXECLTS

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APPENDIX C

THE CIRCUIT ELEMENTS

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M2 (4+1) *R=100E3
M3 (4+0) *R=2.2E3
M4 (2+0) *R=47E3
M5 (5+3) *R=47E3
M6 (0+5) *R=220
M7 (0+6) *R=10E3+E=1
M8 (6+1) *C=1E-6
M9 (4+1) *C=47E-12
M10 (2+0) *C=4.7E-6
M11 (5+0) *C=60E-6

C1 2N930
B12 N(1+7) *R=600
B13 N(7+2) *R=150
B14 N(3+7) *R=1E6
T1 P(12+14) *BETA=170
B15 N(1+3) *C=9E-12

C2 2N930
B16 N(3+8) *R=600
B17 N(8+4) *R=6
B18 N(5+8) *R=1E6
T2 P(16+18) *PFTA=220
B19 N(3+5) *C=9E-12

FREQUENCY=1E3
PRINT VOLTAGES
EXECUTE

FREQ = 0.99999999E 03

NODES NODE VOLTAGES

MAG 1= 4 0.35193714E-01 0.75729779E-02 0.95088840E 01 0.94705141F 01
MAG 5= 8 0.11080429E-01 0.41701452E-01 0.94395122E-01 0.94969132F 01
PHA 2= 4 -0.12766499E 02 -0.90298733E 02 -0.17943960F 03 0.17943946E 03
PHA 5= 8 -0.89836828E 02 -0.33704266E 02 -0.13059527F 02 0.17943956E 03
USL Tech Memo
No 2134.4-597-67

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APPENDIX D

FCAP: IMA 704, A FILIPPINI CODE 2134.4 X 470
DEMONSTRATION AMPLIFIER
RUN 1, 25 JANUARY 1967
INITIAL VOLTAGES DERIVED FROM DC ANALYSIS OUTPUT DATA

TRANSIENT ANALYSIS 0680

THE CIRCUIT ELEMENTS
R1  N(1x0) *R=390E3
R2  N(4x1) *R=100F3
R3  N(4x0) *R=2.2F3
R4  N(2x0) *R=47E3
R5  N(5x3) *P=47E3
R6  N(0x5) *R=220+E=25
R7  N(0x6) *R=10E3
E7  N(1x0) *V=0.0x0 E=0.0x0 E=0.0x0 E=0.0x0 E=0.0x0
B8  N(6x1) *C=1E=6+*E=9x*E=8*51402
B9  N(4x1) *C=47E=12+*E=2.6274608
B10 N(2x0) *C=4.7E=6+*E=9*2714269

C

C
G1  N(2x930
B11 N(1x7) *R=2E3
B12 N(7x2) *R=(22.4E3+10E6)*E=0.55
S1  R=12x)(12)*ON
B13 N(7x2) *R=(10E6+2.54E3)*E=0.614
S2  R=13x)(13)*OFF
B14 N(7x2) *R=(10E6+11)*E=0.63
S3  R=14x)(14)*OFF
B15 N(8x2) *R=100
B16 N(8x3) *R=(2E6+1)
S4  R=16x)(16)*OFF
B17 N(3x8) *R=2E6
T1  R=11x)(17)*BETA=220
B18 N(1x3) *C=9.12=E=9*3147158

C

C
G2  N(2x930
A19 N(3x9) *R=2E3
R20 N(9x4) *R=(22.4E3+10E6)*E=0.55
S5  R=20x)(12)*ON
B21 N(9x4) *R=(2.54E3+10E6)*E=0.614
S6  R=21x)(21)*ON
R22 N(9x4) *R=(1+10E6)*E=0.63
S7  R=22x)(22)*ON
R23 N(10x4) *R=100
R24 N(10x5) *R=(2E6+1)
S8  R=24x)(24)*OFF
R25 N(5x10) *R=2E6
T2  R=19x)(25)*BETA=170
R26 N(3x5) *C=9E=12+E=10*5363160

C
TIME STEP = 10E9
OUTPUT INTERVAL = 100
FINAL TIME = 20E-6
PRINT VOLTAGES
EXECUTE

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APPENDIX E

Outline of this Memorandum

I INTRODUCTION

A. Contents of Memo
B. Purpose of Memo

II SECTION I: PROGRAM DESCRIPTION

A. Purpose of ECAP
B. Three Programs in One
   1. DC Analysis Program
   2. AC Analysis Program
   3. Transient Analysis Program
C. Usefulness of ECAP

III SECTION II: PROGRAMMING SOFTWARE

A. Two Forms are used
   1. Production Request
   2. Fortran Coding Form
B. Punch Cards Used
   1. Time Cards
   2. Comment Cards
      a. Line Spaces, etc.
      b. Identification Cards
   3. Command Cards
      a. AC Analysis Card
      b. DC Analysis Card
      c. Transient Analysis Card
      d. Execute Card
      e. Modify Card
   4. Data Cards
      a. The Standard Brach
      b. B-Cards
      c. T-Cards
      d. M-Cards
      e. S-Cards
      f. Source Cards
         (1) Non-Periodic
         (2) Periodic
         (3) Sinusoidal
g. Use of Data Cards
h. Continuation Cards
i. Limitations on Data Cards
j. Maximum: 50 Nodes
k. Modified Data Cards

5. Solution Control Cards
   a. For AC Analysis
      (1) Frequency Card
      (2) Modified Frequency Card
   b. For DC Analysis
      (1) Sensitivity Card
      (2) Worst Case Card
      (3) Standard Deviation Card
   c. For Transient Analysis
      (1) Time Step Card
      (2) Output Interval Card
      (3) Initial Time Card
      (4) Final Time Card
      (5) Equilibrium Card
      (6) Short Card
      (7) Open Card
      (8) Error Card
      (9) 2 Error Card
      (10) 3 Error Card

6. Output Specification Cards
   a. For AC and DC Analysis
      (1) Print Node Voltages
      (2) Print Element Voltages
      (3) Print Branch Voltages
      (4) Print Element Currents
      (5) Print Branch Currents
      (6) Print Element Power Dissipation
      (7) Print Miscellaneous Outputs
   b. For Transient Analysis
      (1) Print Node Voltages
      (2) Print Element Currents

IV SECTION III: COMPUTING PROCEDURE

A. Recommended Procedure
B. Demonstrate Procedure
   1. DC Bias Point Analysis
      a. Draw DC Diagram
      b. Model Non-Linear Devices
      c. Document ECAP Data
      d. Assist Computer Center Personnel
(1) Have Cards Punched
(2) Assemble Card Deck
(3) Fill in Production Log
(4) Submit Data Cards
(5) Retrieve Output Data

2. DC Worst Case Analysis
3. AC Analysis (Frequency Response)
4. Transient Analysis (Step Response)

V SUMMARY
A. Restate Purpose of Memo
B. Restate Purpose of ECAP

VI REFERENCES

VII FIGURES

VIII APPENDICES